IN THE CLAIMS:

Each claim that remains pending and under consideration in the above-referenced application is reproduced below, in clean form, for the sake of clarity. Also, a marked-up version of each amended claim is enclosed herewith to clearly show each change that has been made thereto.

Please cancel claims 1-37 and 70-74 without prejudice or disclaimer.

Please enter the claims as follows:

38. (Twice amended) A semiconductor device, comprising:

a substrate having contact pads exposed at a surface thereof, said contact pads being arranged in at least one substantially linear relationship positioned at or proximate a centerline of said substrate and being configured to communicate with corresponding test pads of a test substrate upon disposing said substrate face-down over said test substrate; and

at least one stabilizer protruding from said surface, said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device upon disposal thereof face-down over said test substrate.

39. (Twice amended) The semiconductor device of claim 38, wherein said at least one stabilizer protrudes from said surface at most a distance between a plane of said surface of said substrate and a plane of a surface of said test substrate upon disposing said substrate face-down over said test substrate.

40. (Previously amended) The semiconductor device of claim 39, wherein said at least one stabilizer protrudes from said surface at most the distance between said plane of said surface of said substrate and said plane of said surface of said test substrate when at least one conductor connects at least one of said contact pads and a corresponding one of said test pads.

41. The semiconductor device of claim 38, wherein said at least one stabilizer comprises a dielectric material.

42. (Previously amended) The semiconductor device of claim 38, wherein said at least one stabilizer comprises a photopolymer.

43. The semiconductor device of claim 42, wherein said photopolymer is at least semisolid.

44. The semiconductor device of claim 42, wherein said at least one stabilizer has a plurality of superimposed, contiguous, mutually adhered layers.

45. The semiconductor device of claim 38, wherein said at least one stabilizer is positioned to be located proximate a corner of said surface.

46. The semiconductor device of claim 38, wherein said at least one stabilizer is positioned to be located proximate an edge of said surface.

47. The semiconductor device of claim 38, wherein said at least one stabilizer has a cross-sectional plan of one of quadrilateral, round, oval, and triangular.

48. The semiconductor device of claim 38, wherein said at least one stabilizer is elongated.

49. The semiconductor device of claim 38, wherein said substrate comprises a semiconductor wafer.

50. The semiconductor device of claim 38, wherein said substrate comprises a semiconductor die.

51. The semiconductor device of claim 38, wherein said substrate comprises a chip-scale package.

52. (Twice amended) The semiconductor device of claim 38, wherein said test substrate also includes at least one stabilizer configured to at least partially stabilize said substrate upon disposing said substrate face-down over said test substrate.

53. (Twice amended) A test substrate, comprising:

a substrate having test pads exposed at a surface thereof, said test pads being arranged in at least one substantially linear relationship and configured to communicate with corresponding contact pads which are arranged in at least one substantially linear relationship which is positioned at or proximate a centerline of a semiconductor device to be disposed face-down over said substrate; and

at least one stabilizer protruding from said surface, said at least one stabilizer being configured to at least partially stabilize the semiconductor device upon disposal thereof face-down over the test substrate.

54. (Twice amended) The test substrate of claim 53, wherein said at least one stabilizer protrudes from said surface at most a distance between a plane of said surface of said substrate and a plane of a surface of said semiconductor device upon disposing said semiconductor device face-down over said substrate.

55. (Previously amended) The test substrate of claim 54, wherein said at least one stabilizer protrudes from said surface at most the distance between said plane of said surface of said substrate and said plane of said surface of said semiconductor device when at least one conductor connects at least one of said contact pads and a corresponding one of said test pads.

56. The test substrate of claim 53, wherein said at least one stabilizer comprises a photopolymer.

57. The test substrate of claim 56, wherein said photopolymer is at least semisolid.

58. The test substrate of claim 56, wherein said at least one stabilizer comprises a plurality of superimposed, contiguous, mutually adhered layers.

59. The test substrate of claim 53, wherein said semiconductor device has at least one stabilizer secured to a surface thereof, said at least one stabilizer configured to at least partially stabilize said semiconductor device upon disposal of said semiconductor device face-down over said substrate.

60. (Amended) An assembly of a semiconductor device and a test substrate, comprising:

a test substrate with a plurality of test pads exposed at a surface thereof and arranged in at least one substantially linear relationship;

a semiconductor device with a plurality of contact pads exposed at a surface thereof, said plurality of contact pads being arranged in at least one substantially linear relationship which is located at or proximate a centerline of said semiconductor device, said surface of said semiconductor device facing said surface of said test substrate with said plurality of contact pads in communication with corresponding test pads of said plurality of test pads; and

at least one stabilizer disposed between said test substrate and said semiconductor device.

61. The assembly of claim 60, wherein said at least one stabilizer is secured to said surface of said test substrate.

62. The assembly of claim 60, wherein said at least one stabilizer is secured to said surface of said semiconductor device.

63. The assembly of claim 60, comprising a plurality of stabilizers, at least one of said plurality of stabilizers being secured to said surface of said test substrate and at least one other of said plurality of stabilizers being secured to said surface of said semiconductor device.

64. The assembly of claim 60, wherein said at least one stabilizer comprises a photopolymer.

65. The assembly of claim 60, wherein said photopolymer is at least semisolid.

66. The assembly of claim 64, wherein said at least one stabilizer has a plurality of superimposed, contiguous, mutually adhered layers.

67. (Amended) The assembly of claim 60, wherein said at least one stabilizer extends between a plane of said surface of said test substrate and a plane of said surface of said semiconductor device at most a distance between said planes of said surfaces upon establishing communication between said plurality of contact pads and said corresponding test pads.

68. The assembly of claim 60, further comprising at least one conductive structure disposed between said test substrate and said semiconductor device.

69. (Previously amended) The assembly of claim 68, wherein said at least one stabilizer extends between a plane of said surface of said test substrate and a plane of said surface of said semiconductor device at most a distance said at least one conductive structure extends between said planes of said surfaces.